What is claimed is:

1. An integrated circuit comprising:

a substrate;

a connection for receiving an externally supplied voltage having a first upper level; and

a first input transistor having a drain and gate coupled to the connection for reducing the externally supplied voltage and providing an internal voltage having a second upper level at a source of the first input transistor, the first input transistor being fabricated in a first well structure to isolate the input transistor from the substrate such that the first input transistor has an operational breakdown voltage which is less than the first upper voltage level.

2. The integrated circuit of claim 1 wherein the first input transistor is an n-channel transistor fabricated in an isolated p-well.

3. The integrated circuit of claim 1 further comprising:

at least one additional transistor coupled to the source of the first input transistor to further reduce the internal voltage to a third upper level.

4. The integrated circuit of claim 1 further comprising:

a second input transistor having a drain and gate coupled to the source of the first input transistor for reducing the internal voltage to a third upper level at a source of the second input transistor, the second input transistor being fabricated in a second well structure.

5. The integrated circuit of claim 1 further comprising:

a second input transistor having a drain and gate coupled to the source of the first input transistor for reducing the internal voltage to a third upper level at

a source of the second input transistor, the second input transistor being fabricated in the first well structure.

6. An integrated circuit voltage reduction circuit comprising:

an n-well fabricated in an integrated circuit substrate, the n-well having a bottom and side walls;

a p-well fabricated in the n-well;

a first n-channel transistor having a drain and gate coupled to an external connection for receiving an externally supplied voltage, the first n-channel transistor located within the p-well to isolate the first n-channel transistor from the substrate such that the first n-channel transistor has an operational breakdown voltage which is less than the externally supplied voltage level, the first n-channel transistor reduces the externally supplied voltage by an n-channel threshold voltage to provide an internal voltage at a source of the first n-channel transistor; and

a second device coupled to the source of the first n-channel transistor.

7. The integrated circuit voltage reduction circuit of claim 6 wherein the second device is a transistor is an n-channel transistor fabricated in a second p-well.

8. The integrated circuit voltage reduction circuit of claim 6 wherein the second device is an n-channel transistor fabricated in the p-well.

9. The integrated circuit voltage reduction circuit of claim 6 wherein the second device is a p-channel transistor.

10. A flash memory device comprising:

an array of non-volatile memory cells;

a connection for receiving an externally supplied signal having a first upper voltage level;

a voltage reduction circuit having an input coupled to the connection for converting the externally supplied signal to an internal signal available at an output of the voltage reduction circuit, the internal signal having an second upper voltage level which is lower than the a first upper voltage level;

the voltage reduction circuit comprising a first n-channel transistor having a drain and gate coupled to the input of the voltage reduction circuit, the first n-channel transistor is fabricated in an isolated p-well structure and has a source coupled to the output of the voltage reduction circuit; and

an internal circuit coupled to the output of the voltage reduction circuit.

11. The flash memory device of claim 10 wherein the voltage reduction circuit further comprises a second n-channel transistor coupled in series with the first n-channel transistor and fabricated in the isolated p-well structure.

12. The flash memory device of claim 10 wherein the voltage reduction circuit further comprises a second n-channel transistor coupled in series with the first n-channel transistor and fabricated in a second isolated p-well structure.

13. The flash memory device of claim 10 wherein the internal circuit is a flash memory write circuit for coupling the externally supplied signal to the array of non-volatile memory cells for performing a write operation.

14. The flash memory device of claim 10 wherein the internal circuit is a flash memory erase circuit for coupling the externally supplied signal to the array of non-volatile memory cells for performing a erase operation.

15. A processing system comprising:

a controller coupled to a memory device for bi-directional data communication; and

the memory device comprising,

a substrate;

a connection for receiving an externally supplied voltage having a first upper level; and

a first input transistor having a drain and gate coupled to the connection for reducing the externally supplied voltage and providing an internal voltage having a second upper level at a source of the first input transistor, the first input transistor being fabricated in a first well structure to isolate the input transistor from the substrate such that the first input transistor has an operational breakdown voltage which is less than the first upper voltage level.

16. The processing system of claim 15 wherein the first input transistor is an n-channel transistor fabricated in an isolated p-well.

17. A voltage regulator circuit comprising:

a connection for receiving an externally supplied voltage having a first upper level;

a first voltage reduction circuit comprising a first diode coupled transistor coupled to receive the externally supplied voltage from the connection for reducing the externally supplied voltage and providing a first internal voltage having a second upper level;

a second voltage reduction circuit comprising a second transistor coupled to receive the externally supplied voltage from the connection for receiving the

externally supplied voltage and providing a second internal voltage at a source of the second transistor;

a switching circuit coupled to the first and second voltage reduction circuits, the switching circuit couples a gate of the second transistor to the first internal voltage in response to a first enable signal state, and couples the gate of the second transistor to a deactivation voltage in response to a second enable signal state.

18. The voltage regulator circuit of claim 17 wherein the first diode coupled transistor is an n-channel transistor fabricated in an isolated p-well.

19. The voltage regulator circuit of claim 17 wherein the first diode coupled transistor is a p-channel transistor fabricated in an isolated n-well.

20. The voltage regulator circuit of claim 17 wherein the first voltage reduction circuit further comprises a third transistor coupled as a diode.

21. The voltage regulator circuit of claim 17 wherein the second transistor is an n-channel transistor fabricated in an isolated p-well.